BitWatts: A Process-level Power Monitoring Middleware

Maxime Colmant, Mascha Kurpicz, Pascal Felber, Loïc Huertas, Romain Rouvoy, Anita Sobe

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Motivation

- Create software-defined power meters
- Identify the largest power consumers
- Provide critical indicators
- Make informed decisions (heuristics, power capping)
- Provide architecture-agnostic solutions
- Limited number of power-aware interfaces (RAPL)

Metrics

Hardware Performance Counter (HPC):

- Representative and accurate metrics
- Mostly available on modern processors

Criteria selection:

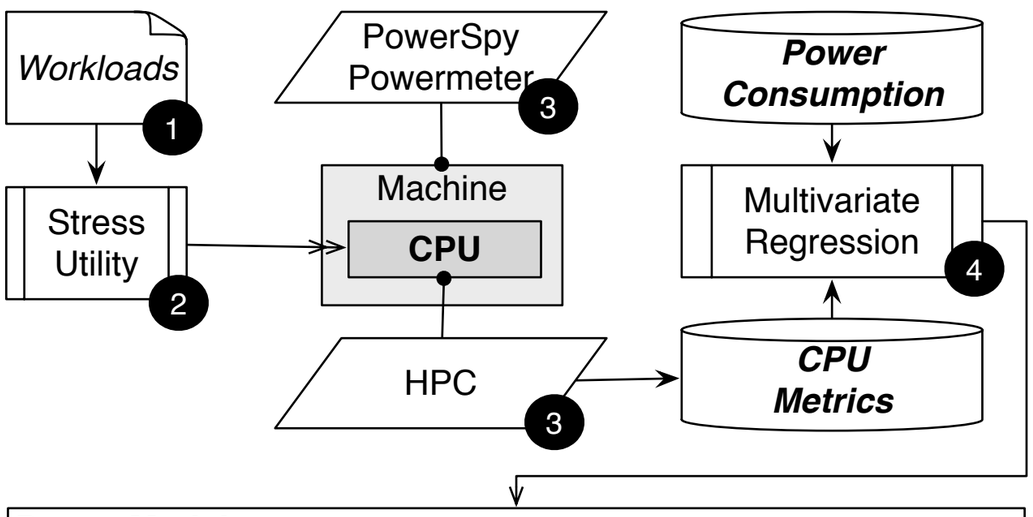
- Counter availability per CPU
- Monitoring overhead
- Best fit under several workloads

Selected HPC:

- `instructions (i), cache-references (r), cache-misses (m)`

BitWatts Middleware

Learning the CPU Power Model

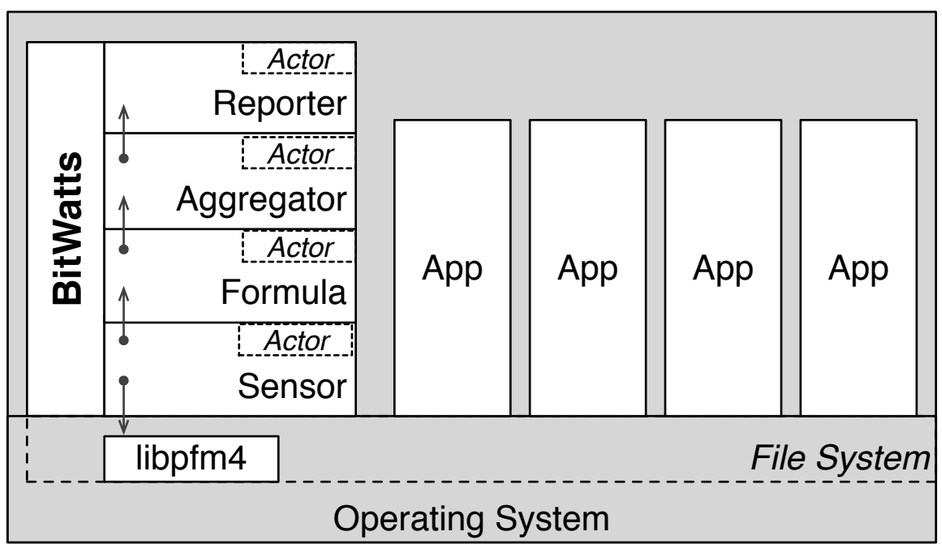


Power Model

$$Power_{Xeon} = 90.23 + \sum_{\substack{f=1.6,\\ f \in Freq}}^{2.93} Power_f$$

$$Power_{2.93} = \frac{5.37 \cdot i}{10^9} + \frac{7.67 \cdot r}{10^8} + \frac{3.23 \cdot m}{10^7}$$

Architecture



- Actor programming model (Scala / Akka)
- Modular & Scalable Middleware
- Real-time power estimation (10Hz-100Hz)

Preliminary experiment

Conclusion

A Middleware to build software-defined power meters

- High-level power API
- Processor-agnostic solution
- Power-model inference by sampling
- Real-time power estimation

Outlook

- Support AMD, ARM
- Support virtualized environments
- Identify automatically the HPCs
- Heuristics, power capping

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